What is claimed is:

1. A circuit for handling pulse width modulation (PWM) first signal and PWM second signal for outputting to an amplifier, the PWM first signal having one of a same phase and an opposite phase relationship with the PWM second signal, the circuit comprising:

a power detector for detecting power turn on to the amplifier and outputting a power on signal; and

a pulse generator having: a duty cycle generator for generating a first pulse signal corresponding to the PWM first signal and a second pulse signal corresponding to the PWM second signal; and a pulse reducing generator for generating a reduced-width first pulse or a reduced-width second pulse for outputting to the amplifier upon receipt of the power on signal.

2. The circuit of claim 1, wherein the pulse generator further includes a controller for outputting the reduced-width first pulse or the reduced-width second pulse upon receipt of the power on signal and for outputting the first pulse signal and the second pulse signal to the amplifier thereafter.

3. The circuit of claim 1, further including a select circuit for generating a select signal for selecting between the PWM first and second signals during one selection mode and the signals from the pulse generator during another selection mode.

4. The circuit of claim 3, further including a counter for counting time upon receipt of the power on signal and to output the select signal in the another selection mode upon reaching a predetermined count for outputting the PWM first and second signals to the amplifier.

5. The circuit of claim 1, wherein the reduced-width first pulse is about one-half the pulse width of the first pulse signal.

6. The circuit of claim 1, further including a delay for delaying by a predetermined time the first pulse signal to output a delayed first pulse signal that transitions with a delay by the predetermined time to provide a time gap between the transition of the delayed first pulse signal and the transition of the second pulse signal.

7. The circuit of claim 1, wherein the amplifier includes a serially connected pair of transistors for receiving at their gates the first pulse signal and the second pulse signal.

8. A circuit for handling pulse width modulation (PWM) first signal and PWM second signal for outputting to an amplifier, the PWM first signal having one of a same and an opposite phase relationship with the PWM second signal, the circuit comprising:

a power detector for detecting power turn off to the amplifier and outputting a power off signal; and

a counter for counting the duration of the pulse width of the PWM first signal, the counter being activated upon detection of the power off signal, and for outputting a select signal upon reaching a predetermined reduced-width time count to cause an output of a reduced pulse width PWM first signal or reduced pulse width PWM second signal prior to complete power turn off from the amplifier.

9. The circuit of claim 8, further including a synchronizing circuit for synchronizing the power off signal using a system clock.

10. The circuit of claim 8, wherein the amplifier includes a pair of transistors for receiving at their gates the PWM first signal and the PWM second signal.

11. The circuit of claim 8, further including a mute circuit for outputting the select signal to cause an output of a reduced pulse width PWM first signal or reduced pulse width PWM second signal upon receipt of a mute signal.

12. The circuit of claim 11, wherein the mute circuit is an AND gate.

13. The circuit of claim 12, wherein the reduced pulse width PWM first signal or reduced pulse width PWM second signal is the last pulse signal received by the amplifier prior to complete power turn off.

14. The circuit of claim 10, wherein the reduced-width is about one half of the width of the PWM first signal or the PWM second signal.

15. A circuit for handling pulse width modulation (PWM) first signal and PWM second signal for outputting to an amplifier, the PWM first signal having one of a same phase and an opposite phase relationship with the PWM second signal, the circuit comprising:

a power detector for detecting power turn on to the amplifier and outputting a power on signal and detecting a power turn off to the amplifier and outputting a power off signal;

a pulse generator having: a duty cycle generator for generating a first pulse signal corresponding to the PWM first signal and a second pulse signal corresponding to the PWM second signal, and a reduced-width generator for generating at least one of a reduced-width first pulse and a reduced-width second pulse;

a controller for selecting one of the reduced-width first pulse and the reduced-width second pulse for outputting to the amplifier upon receipt of the power on signal and for selecting the first pulse signal and the second pulse signal for outputting to the amplifier thereafter; and

a counter for counting the duration of the pulse width of the PWM first signal, the counter being activated upon detection of the power off signal and a select circuit for outputting an off select signal upon reaching a predetermined reduced-width time count to cause an output of one of a reduced-width PWM first signal and a reduced-width PWM second signal.

16. The circuit of claim 15, wherein the select circuit further includes a counter for counting time upon receipt of the power on signal and to output an on select signal for first outputting one of the reduced-width first pulse and the reduced-width second pulse and then the first pulse signal and the second pulse signal to the amplifier.

17. The circuit of claim 15, further including a mute circuit for outputting the on select signal for outputting one of the reduced-width first pulse and the reduced-width second pulse to the amplifier upon receipt of a mute signal.

18. The circuit according to claim 17, wherein the mute circuit is synchronized using a system clock and upon mute inactivation, to cause an output of one of the reduced-width PWM first signal and the reduced-width PWM second signal.

19. The circuit according to claim 15, wherein the reduced-width first pulse signal has a pulse width about one half of the pulse width of the first pulse signal.

20. The circuit according to claim 15, wherein the predetermined reduced-width time count is about one half the duration of the pulse width of the PWM first signal.

21. The circuit of claim 15, further including a delay for delaying by a predetermined time the first pulse signal to output a delayed first pulse signal that transitions with a delay by the predetermined time to provide a time gap between the

transition of the delayed first pulse signal and the transition of the second pulse signal.

22. The circuit of claim 21, wherein the amplifier includes a pair of transistors for receiving at their gates the delayed first pulse signal and the second pulse signal.

23. The circuit of claim 15, wherein the amplifier includes a pair of transistors for receiving at their gates the first pulse signal and the second pulse signal.

24. A method for handling pulse width modulation (PWM) first signal and PWM second signal for outputting to an amplifier, the PWM first signal having one of a same phase and an opposite phase relationship with the PWM second signal, the method comprising:

detecting power turn on to the amplifier and outputting a power on signal; and

generating a first pulse signal corresponding to the PWM first signal and a second pulse signal corresponding to the PWM second signal; and

generating a reduced-width first pulse or a reduced-width second pulse for outputting to the amplifier upon receipt of the power on signal.

25. The method of claim 24, further including outputting the reduced-width first pulse or the reduced-width second pulse to the amplifier upon receipt of the power on signal and outputting the first pulse signal and the second pulse signal to the amplifier thereafter.

26. The method of claim 24, further including generating a select signal for selecting between the PWM first and second signals during one selection mode and the first pulse signal and the second pulse signal during another selection mode for outputting to the amplifier.

27. The method of claim 24, wherein the reduced-width first pulse is about one-half the pulse width of the first pulse signal.

28. The method of claim 24, further including delaying by a predetermined time the first pulse signal to output a delayed first pulse signal that transitions with a delay by the predetermined time to provide a time gap between the transition of the delayed first pulse signal and the transition of the second pulse signal.

29. The method of claim 24, further including the steps of:

detecting power turn off to the amplifier and outputting a power off signal;

counting the duration of the pulse width of the PWM first signal upon detection of the power off signal; and

outputting a select signal upon reaching a predetermined reduced-width time count to cause an output of a reduced pulse width PWM first signal or reduced pulse width PWM second signal prior to complete power turn off from the amplifier.

30. The method of claim 24, wherein the reduced pulse width PWM first signal or reduced pulse width PWM second signal is the last pulse signal received by the

amplifier prior to complete power turn off.

31. The method of claim 24, wherein the reduced-width is about one half of the width of the PWM first signal or the PWM second signal.

32. The method of claim 24, further including outputting the select signal to cause an output of a reduced pulse width PWM first signal or reduced pulse width PWM second signal upon receipt of a mute signal.

33. A circuit for handling pulse width modulation (PWM) first signal and PWM second signal for outputting to an amplifier, the PWM first signal having one of a same phase and an opposite phase relationship with the PWM second signal, the circuit comprising:

means for detecting power turn on to the amplifier and outputting a power on signal and detecting a power turn off to the amplifier and outputting a power off signal;

means for generating a first pulse signal corresponding to the PWM first signal and a second pulse signal corresponding to the PWM second signal, and a reduced-width generator for generating at least one of a reduced-width first pulse and a reduced-width second pulse;

means for selecting one of the reduced-width first pulse and the reduced-width second pulse for outputting to the amplifier upon receipt of the power on signal and for selecting the first pulse signal and the second pulse signal for outputting to the amplifier thereafter; and

a counter for counting the duration of the pulse width of the PWM first signal, the counter being activated upon detection of the power off signal and a select circuit for outputting an off select signal upon reaching a predetermined reduced-width time count to cause an output of one of a reduced-width PWM first signal and a reduced-width PWM second signal.